M-Systems
Flash Disk Pioneers

Abstract

Overcoming the Reliability and Performance Barriers of Low-Cost Flash MLC Technology

As OEMs scramble to bring to market reliable and high-performance advanced computing systems at a price that suits today's cautious economic environment, many are weighing the benefits and cost of every component. The more functionality that OEMs offer users to support applications such as moving maps, tactical computers and airborne systems, the more memory capacity that is required to store additional applications and user data – reliably, cost-effectively, and space-effectively. To meet these demands, OEMs are encouraging flash memory manufacturers to implement advanced technologies that can provide the performance and reliability of a big system in a low-cost, small-as-possible package.

Among the technologies that flash memory manufacturers are investigating is Multi-Level Cell (MLC) technology. While standard flash technology can only store one bit per cell, MLC technology offers double the bit storage capacity per cell. Storing two data bits in a single physical cell significantly reduces the total die size, which has a major impact on the silicon cost since one of the major factors determining silicon cost is the die area.

On the surface, MLC looks like the perfect solution. But without highly reliable and efficient algorithms to guarantee data reliability, and some mechanism to boost MLC performance, which is much lower than standard NAND-based performance, MLC technology can meet neither reliability nor performance requirements.

To overcome these obstacles and deliver a low-cost MLC solution, M-Systems recently partnered with well-established OEM flash manufacturer Toshiba. Working closely with Toshiba, M-Systems developed a breakthrough technology to enable MLC as a local memory storage solution, without compromising reliability and achieving performance rates that rival standard NAND-based flash technology rates. DiskOnChip NAND-based MLC, engineered with M-Systems' proprietary x2 technology, uses a patented, sequential-access flash translation layer scheme for more robust code and data storage management, MultiBurst mode for performance acceleration, enhanced, hardware-based on-the-fly error detection that does not reduce system performance, and software-based error correction, when required, to save silicon costs. x2 technology is implemented in a single-die chip, including both the flash array and the flash controller packed in a minimal, 9x12mm Ball Grid Array (BGA) package. This cost-effective and space-saving architecture, when combined with MLC's low-cost structure, may very well make DiskOnChip NAND-based MLC the memory breakthrough that OEMs have been seeking.

This presentation will discuss the growing need for high-performance and high-reliability flash memory in large capacities, the evolution of popular flash technologies to meet this need, the advantages and tradeoffs of MLC solutions available on the market today, and the revolutionary architecture and benefits that make DiskOnChip NAND-based MLC such a promising new technology.

Proposed Speaker's Bio

Raz Dan is the Director of Technology for M-Systems Inc., Newark, Calif., a company that has been pioneering storage solutions based on flash memory and TrueFFS technology for over thirteen years. Currently responsible for promoting the company's hardware and software technology, he helps customers integrate these products into new designs on a daily basis. Mr. Dan has been involved in the design and implementation of flash disks for ten years. Prior to joining M-Systems, he worked as both a software and hardware engineer on various types of embedded systems.

Mr. Dan received his B.Sc. in Electrical Engineering in 1990 from Tel Aviv University, Israel. He may be reached at: raz.dan@m-sys.com.